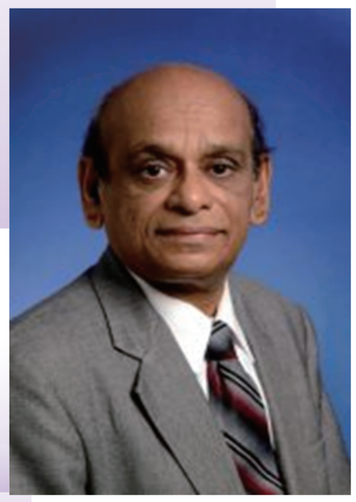
『清华信息大讲堂第102讲-NEC第6讲』



报告题目： Cross-Layer Survivability in a Layered Network

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摘　要：

An IP-over-WDM optical network is an example of a layered network. In this network, the grapah representing the optical network is called the physical topology GP and the graph representing the IP layer is called the logical topology GL. Without loss of generality, we assume that GL has the same set of nodes as GP . Each logical link (i,j) is associated with a path incurrent connecting the nodes i and j. Such a path is called a lightpath. The survivable logical topology mapping problem in a layered network is to map each link (u, v) in the logical topology into a lightpath between the nodes u and v in the physical topology such that failure of a physical link does not cause the logical topology to become disconnected. It is assumed that both the physical and logical topologies are 2-edge connected. This mapping problem also arises in other areas of applications such as the problem of mapping a parallel program onto a multiprocess system, though the constraints there are of a different type.

For the survivable logical mapping problem, two lines of investigations have been pursued in the literature: mathematical programming based approach pioneered by Modiano et al., and the structural approach pioneered by Kurant and Thiran. Kurant and Thiran presented an algorithmic framework called SMART that involves successively contracting circuits in the logical topology, and mapping the logical links in the circuits into edge disjoint lightpaths in the physical topology. In a recent work, we presented a dual framework involving cutsets and showed that both these frameworks possess the same algorithmic structure. In a series of papers, we have developed several versions of this framework with varying degrees of robustness in providing survivability against multiple failures. We have also investigated several issues related to the sturctural survivability of logical topology, as well as augmenting a logical topology with additional links that guarantees the existence of a survivable mapping. In this lecture we will present a review of these results and some of our research directions in this area.

简　介：

Krishnaiyan Thulasiraman received the Bachelor’s degree (1963) and Master’s degree (1965) in Electrical Engineering from the College of Engineering, Guindy (University of Madras, India)and the Ph.D. degree (1968) in Electrical Engineering from IIT, Madras, India. He holds the Hitachi Chair and is Professor in the School of Computer Science at the University of Oklahoma, Norman, where he has been since 1994. Prior to joining the University of Oklahoma, Thulasiraman was professor (1981-1994) and chair (1993-1994) of the ECE Department in Concordia University, Montreal, Canada. He was on the faculty in the EE and CS departments of the IITM during 1965-1981.

Dr. Thulasiraman’s research interests have been in graph theory, combinatorial optimization, algorithms and applications in a variety of areas in CS and EE: electrical networks, VLSI physical design, systems level testing, communication protocol testing, parallel/distributed computing, telecommunication network planning, fault tolerance in optical networks, interconnection networks etc. He has published extensively in archival journals, coauthored with M. N. S. Swamy two text books “Graphs, Networks, and Algorithms” (1981) and “Graphs: Theory and Algorithms” (1992), both published by Wiley Inter-Science.

Dr. Thulasiraman has received several awards and honors: Distinguished Alumnus Award of IIT Madras(2008), Fellow of the American Association for Advancement of Science (2007), 2006 IEEE Circuits and Systems Society Charles Desoer Technical Achievement Award. Endowed Gopalakrishnan Chair Professorship in CS at IIT, Madras (Summer 2005), Fellow of the European Academy of Sciences (2002), IEEE CAS Society Golden Jubilee Medal (1999), Fellow of the IEEE (1990) and Senior Fellow of the Japan Society for Promotion of Science (1988). He has held visiting positions at the Tokyo Institute of Technology, University of Karlsruhe, University of Illinois at Urbana-Champaign and Chuo University, Tokyo, University of Waerloo and the National Chia0-Tung University, Taiwan.

Dr. Thulasiraman has extensive experience in collaborative research involving multiple research teams and universities . He was a principal investigator for the VLSI and Telecommunication teams at the provincial and national level, while working in Monreal, Canada. He was one of the four co-founders of the Montreal (Quebec) inter-university centre on Microelectronics and Computer Architectures called RESMIQ, that ceoebrated its 25th anniversary in June 2012. He has served as editor of several journals and asTechnical Program Chair of ISCAS 1993 and 1999. He has served as aVice Pesident of the IEEE Circuits and Systems Society.

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